IN THE CLAIMS

1. (Currently Amended) An apparatus comprising:

~~a memory~~one or more memory devices, ~~to~~ coupled to a data bus, to receive a command signal~~to transfer data between said memory and bus in response to a command signal~~, wherein the command signal initiates ~~received to initiate the~~ a plurality of data transfer operations to transfer data between the data bus and one of the one or more memory devices~~and a flag signal received to complete the data transfer~~; and

a timing unit, coupled to the one or more memory devices, to receive the command signal, a flag signal, and a memory select signal, said timing unit to generate a trigger signal, in response to a transition of the flag signal, to ~~execute the data transfer~~complete the plurality of data transfer operations~~,~~ if ~~the command signal indicates a command to transfer data and~~ the memory select signal ~~indicates that said memory is selected for the data transfer~~corresponds to the one of the one or more memory devices.

2. (Currently Amended) The apparatus of claim 1, wherein said timing unit includes a table having one or more table entries ~~entry~~ to maintain a record of the command signal, the memory select signal, and the flag signal, so that an indication of a presence of all three signals causes the trigger signal to be generated ~~to execute the data transfer~~.

3. (Currently Amended) The apparatus of claim 2, wherein the table includes a storing information entry corresponding to the trigger signal generated that ~~is to be~~ cleared after receiving the flag signal to allow said table entry to receive a next set of command, memory select, and flag signals to determine if the trigger signal is to be

generated for ~~said~~ one of the plurality of memory devices with the next set of command, memory select, and flag signals.

4. (Currently Amended) The apparatus of claim 3, wherein the transition of the flag signal ~~to indicate timing of the data transfer occurs with~~may be a positive ~~and~~ transition or a negative transitions ~~of the flag signal~~.

5. (Currently Amended) The apparatus of claim 3, wherein ~~said memory is a~~the one or more memory devices include one or more dynamic random access memories (DRAM) ~~dynamic random access memory, DRAM~~.

6. (Currently Amended) The apparatus of claim ~~1~~2, wherein ~~said timing unit includes~~the one or more table entries are arranged in a queue ~~to maintain record of occurrences of the command signal, memory select signal and the flag signal, so that an indication of a presence of all three signals for a given set of command, memory select and flag signals are recorded in a given set of entries and causes the trigger signal to be generated to execute the data transfer~~.

7. (Currently Amended) The apparatus of claim 6, wherein the timing unit further includes a first pointer to point to a next set of table entries after recording ~~the~~ an occurrence of the command and memory select signals~~;~~, and a second pointer to point to the next set of entries after recording ~~the~~ an occurrence of the flag signal.

8-11. Canceled.

12. (Currently Amended) The apparatus of claim ~~11~~ 1, wherein the command signal ~~is~~ may be a read command or write command.

13-19. Canceled.

20. (Currently Amended) A system comprising:

a bus;

a controller to generate a command signal, ~~to initiate data transfer and also to generate~~ a flag signal, and a chip select signal ~~to time completion of the data transfer~~; and

a memory unit, coupled to said controller via the bus, the memory unit including one or more memory devices to receive the command signal, wherein the command signal initiates a plurality of data transfer operations to transfer data between the bus and one of the one or more memory devices; and

a timing unit, coupled to the one or more memory devices, to receive the command signal, the flag signal, and the chip select signal, the timing unit to generate a trigger signal in response to a transition of the flag signal to complete the plurality of data transfer operations if the chip select signal corresponds to the one of the one or more memory devices. ~~and complete the data transfer in response to the flag signal;~~

~~a bus coupled to said memory to transfer data between said memory and bus in response to the flag signal;~~

~~said controller to generate the command signal during a first clock period, along with a corresponding chip select signal to activate said memory to perform the data transfer, and the flag signal following the data transfer command signal at a later clock period; and~~

~~said memory including a timing unit coupled to receive the command signal, flag signal and a chip select signal, said timing unit to generate a trigger signal in response to the flag signal to execute the data transfer, if the command signal indicates the data transfer and the chip select signal indicates that said memory is selected for the data transfer.~~

21. (Currently Amended) The system of claim 20, wherein said timing unit includes a table ~~table entries~~ to maintain a record of the command signal, the chip select signal, and the flag signal, so that a command entry in the table is to be set when the ~~read or write~~ command signal is present, a chip select entry in the table is to be set when the chip select signal is present, and the flag entry in the table is to be set when the flag signal is present, the trigger signal to be generated to ~~execute~~ complete the plurality of data transfer operations when all three respective entries are set.

22. (Currently Amended) The system of claim 21, wherein the respective ~~table~~ entries in the table are to be cleared after receiving the flag signal to allow the entries to receive a next set of command, chip select, and flag signals.

23. (Currently Amended) The system of claim 22, wherein the transition of the flag signal ~~to indicate timing of the data transfer occurs with~~ may be a positive ~~and~~ transition or a negative transitions ~~of the flag signal~~.

24. (Currently Amended) The system of claim 22, wherein ~~said memory is a dynamic random access memory, DRAM~~the one or more memory devices include one or more dynamic random access memories (DRAM).

25. (Currently Amended) A method comprising:

issuing a command signal to ~~perform a read or write~~initiate a plurality of data transfer operations;

issuing a chip select signal to select one of a ~~particular~~ plurality of memory devices ~~to perform a data transfer for the read or write operation~~;

generating a flag signal subsequent~~ly~~ to the issuing of the command signal and the issuing of the chip select signal~~in response to the issuing of the command signal to completes the data transfer~~; ~~and~~

capturing an occurrences of each of the command signal, the chip select signal, and the flag signal in ~~a~~ the selected memory device; and

generating a trigger signal when the command, chip select, and flag signals present are captured for the selected memory device, the trigger signal to ~~execute the data transfer to~~ complete the ~~read or write~~plurality of data transfer operations ~~in~~ on the selected memory device.

26. (Original) The method of claim 25 wherein the command signal is driven in a same clock period the chip select signal is asserted.

27. (Currently Amended) The method of claim 26, wherein said capturing the occurrence of each of the command, chip select, and flag signals ~~are achieved by~~comprises setting ~~entries on occurrence of the signals~~an entry for the corresponding signal in a table.

28. (Currently Amended) The method of claim 27, further including ~~the~~ clearing ~~of~~ the entries corresponding to the command, chip select, and flag signals after the occurrence of the flag signal.

29. (Currently Amended) The method of claim ~~26~~25, wherein ~~said capturing of the signals is performed in a dynamic random access memory, DRAM~~the plurality of memory devices includes one or more dynamic random access memories (DRAM).